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AMENDMENTS TO THE CLAIMS

This listing and version of the claims replace all prior listings and versions of the claims.

Listing of Claims:

1-31. (Canceled)

32. (Currently amended) An integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground for preventing electrostatic discharge damage to said integrated circuit comprising:

a first semiconductor layer having a first conductivity dopant type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant concentration;

a third semiconductor layer having a second conductivity dopant type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopant type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer; and

a plurality of third regions of said first semiconductor layer conductivity dopant type laterally spaced and interposed between said second regions,

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wherein said third regions are alternatingly arranged in an array within said third semiconductor layer, wherein, when ~~with~~ "N" by definition is the number of said third regions, ~~whereby "N" is the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure~~ said third regions are electrically connected by a conductor element to N horizontal stripe conductor elements, at least two of said horizontal stripe conductor elements are connected by at least one first contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at one end of said horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one second contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at another end of the horizontal stripe conductor elements so that said horizontal stripe conductor elements are electrically connected to each other, and

wherein one of said second regions of said second conductivity dopant type is disposed between said array and a ~~top~~first one of said first regions and, ~~and~~ another of said second regions is disposed between said array and a ~~bottom~~second one of said first regions, and said first one of said first regions and said second one of said first regions are disposed on laterally opposite ends of said plurality of said first regions.

33. (Previously presented) The ESD protection structure of claim 32 whereby the plurality of said first regions together with the associated connected first semiconductor layer are with n dopant and form multiple collector elements of a bipolar transistor in which the bases are formed by said third semiconductor layer and associated with said plurality of said second regions of p dopant, and by which multiple emitter elements are formed by said plurality of third regions of n type dopant.

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34. (Canceled)

35. (Currently amended) The ESD protection structure of claim 32 whereby said first regions have horizontal contact conductor stripes at ~~the top~~a first end and ~~bottom~~a second end of said transistor array which are laterally, oppositely disposed and are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

36. (Canceled)

37. (Currently amended) The ESD protection structure of claim 32 whereby said third regions are electrically connected by ~~a~~said conductor element with said N horizontal stripe conductor elements and connected in a contiguous box shaped manner by said~~vertical~~ contact conductor elements at both ends of said horizontal emitter conductor stripes.

38. (Previously presented) The ESD protection structure of claim 32 whereby said second regions and said third regions are ultimately connected together and to a second voltage source.

39-46. (Canceled)

47. (Previously presented) The ESD protection structure of claim 38, wherein the second voltage source is ground.

48. (Canceled)

49. (Currently amended) An integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate, comprising:

an n+-type semiconductor layer;

an n-type semiconductor layer overlying the n+-type semiconductor layer;

a p-type semiconductor layer disposed in overlying relation to the n-type semiconductor layer;

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a plurality of first n+-type regions electrically connecting with the n+-type semiconductor layer, having a top element making electrical contact to the first n+-type regions and the n+-type semiconductor layer;

a plurality of p+-type regions laterally spaced from the n+-type regions, being electrically connected to the p-type semiconductor layer having a top element making electrical contact to the p+-type regions and the p-type semiconductor layer; and

a plurality of second n+-type regions laterally spaced and interposed between the p+-type regions,

wherein the second n+-type regions are alternatingly arranged in an array within the p-type semiconductor layer, and ~~with "N"~~a number of the second n+-type regions is represented by "N," whereby~~"N" is the number of multiple bipolar transistors in an electrically parallel transistor array~~ the second n+-type regions are electrically connected by a conductor element with N horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one first contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at one end of said horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one second contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at another end of said horizontal stripe conductor elements so that said horizontal stripe conductor elements are electrically connected to each other, and

wherein one of the p+-type regions is disposed between the array and a ~~top~~first one of the first n+-type regions, ~~and~~ another of the p+-type regions is disposed between the array and a ~~bottom~~second one of the first n+-type regions, and said first one of said first n+-type regions and

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second one of said first +-type regions are disposed on laterally opposite ends of said first n+-type regions.

50. (Previously presented) The ESD protection structure of claim 49, wherein the plurality of the first n+-type regions together with the associated connected n+-type semiconductor layer form multiple collector elements of a bipolar transistor in which the bases are formed by the p-type semiconductor layer and associated with the plurality of the p+-type regions, and by which multiple emitter elements are formed by the plurality of the second n+-type regions.

51. (Currently amended) The ESD protection structure of claim 49, wherein the first n+-type regions have horizontal contact conductor stripes at ~~the top~~a first end and ~~bottom~~a second end of the transistor array which are laterally, oppositely disposed and are ultimately connected together and to a first voltage source of the integrated circuit input/output pin.

52. (Previously presented) The ESD protection structure of claim 49, wherein the second n+-type regions are electrically connected by asaid conductor element with said N horizontal stripe conductor elements and connected in a contiguous box shaped manner by ~~vertical~~said contact conductor elements at both ends of the horizontal emitter conductor stripes.

53. (Previously presented) The ESD protection structure of claim 49, wherein the plurality of the p+-type regions and the second n+-type regions are ultimately connected together and to a second voltage source.

54. (Previously presented) The ESD protection structure of claim 53, wherein the second voltage source is ground.

55. (Canceled)

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